

Release Notes for HDL Verifier™

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Release Notes for HDL Verifier™

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R2013a

FPGA-in-the-loop test bench generation through HDL Workflow Advisor for MATLAB	2
HDL cosimulation test bench generation through HDL Workflow Advisor for MATLAB	3
Transaction Level Model generation using Simulink Coder	4
Support Package for FPGA-in-the-Loop	5
Code Generation for FIL Simulation Block	6
Updates to supported software and boards	7
HDL Verifier No Longer Supports Legacy FIL Programming Files	8
Functions and Function Elements Being Removed	9

R2012b

Custom board APIs for FPGA-in-the-loop	12
System object for FPGA-in-the-Loop	13
100 Base-T Ethernet support for FPGA-in-the-loop block	14
Automatic verification with cosimulation using HDL Coder	15
Updates to supported software and boards	16

R2012a

EDA Simulator Link Is Now HDL Verifier	18
FPGA-in-the-Loop for Altera Boards	19
System Object for HDL Cosimulation with MATLAB, with Automatic System Object Generation	20
Use of FPGA Board as Source Block with FPGA-in-the-Loop	21
HDL Regression Testing with Simulink Design Verifier ..	22

New Examples for R2012a	23
HDL Verifier Supported Software and System Updates ..	24
Functions and Function Elements Being Removed	25

R2011b

FPGA-in-the-Loop Workflow in HDL Coder HDL Workflow Advisor	28
FPGA-in-the-Loop Updates	29
Conversion of Error and Warning Message Identifiers ...	30
EDA Simulator Link Supported Software and System Updates	31
Functions and Function Elements Being Removed	32

R2011a

FPGA-in-the-Loop Simulation	36
Multiple Cosimulation Sessions Support with Parallel Computing	37
New User Guide Section for Using HDL Instance Object with Test Bench and Component Functions	38
EDA Cosimulation Assistant Name Change to Cosimulation Wizard	39
EDA Simulator Link Supported Software and System Updates	40
Functions and Function Elements Being Removed	41

R2010b

HDL Cosimulation Updates	44
FPGA Automation Updates	46
TLM Generation Updates	47

R2010a

Support for Latest Synopsys Discovery Release	50
Enable Direct Feedthrough for HDL Designs with Pure Combinational Datapaths	51
New Functions for HDL Simulator Client Communication	52
Batch, CLI, and GUI Mode Support Added for Cosimulation with HDL Simulators	53
Use Same MATLAB Function for Multiple HDL Instances	54
Generating Transaction Level Models for Use with Virtual Platforms	55
Specializing FPGA Implementations	56

R2009b

EDA Simulator Link DS, EDA Simulator Link IN, and EDA Simulator Link MQ Merge	58
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R2013a

Version: 4.2
New Features: Yes
Bug Fixes: Yes

FPGA-in-the-loop test bench generation through HDL Workflow Advisor for MATLAB

With the MATLAB® Coder™ Workflow Advisor, the HDL Verification step includes automation for the following workflow:

- Verify with FPGA-in-the-Loop: Create the FPGA programming file and test bench, and, optionally, download it to your selected development board.

Note You *do* require an HDL Verifier™ license to use this feature.

HDL cosimulation test bench generation through HDL Workflow Advisor for MATLAB

With the MATLAB Coder Workflow Advisor, the HDL Verification step includes automation for the following workflows:

- Verify with HDL Test Bench: Create a standalone test bench. You can choose to simulate using ModelSim® or Incisive® with a vector file created by the Workflow Advisor.

Note You do not require an HDL Verifier license to use this feature.

- Verify with Cosimulation: Cosimulate the device under test (DUT) in ModelSim or Incisive with the test bench in MATLAB.

Note You *do* require an HDL Verifier license to use this feature.

Transaction Level Model generation using Simulink Coder

Compatibility Considerations: Yes

You can generate Transaction Level Models with either a Simulink® Coder license *or* an Embedded Coder® license. You are not required to have both product licenses.

In Model Configuration Parameters, under **Code Generation**, follow these guidelines for selecting the correct system target file:

- With Simulink Coder, select: `tlmgenerator_grt.tlc`
- With Embedded Coder, select: `tlmgenerator_ert.tlc`

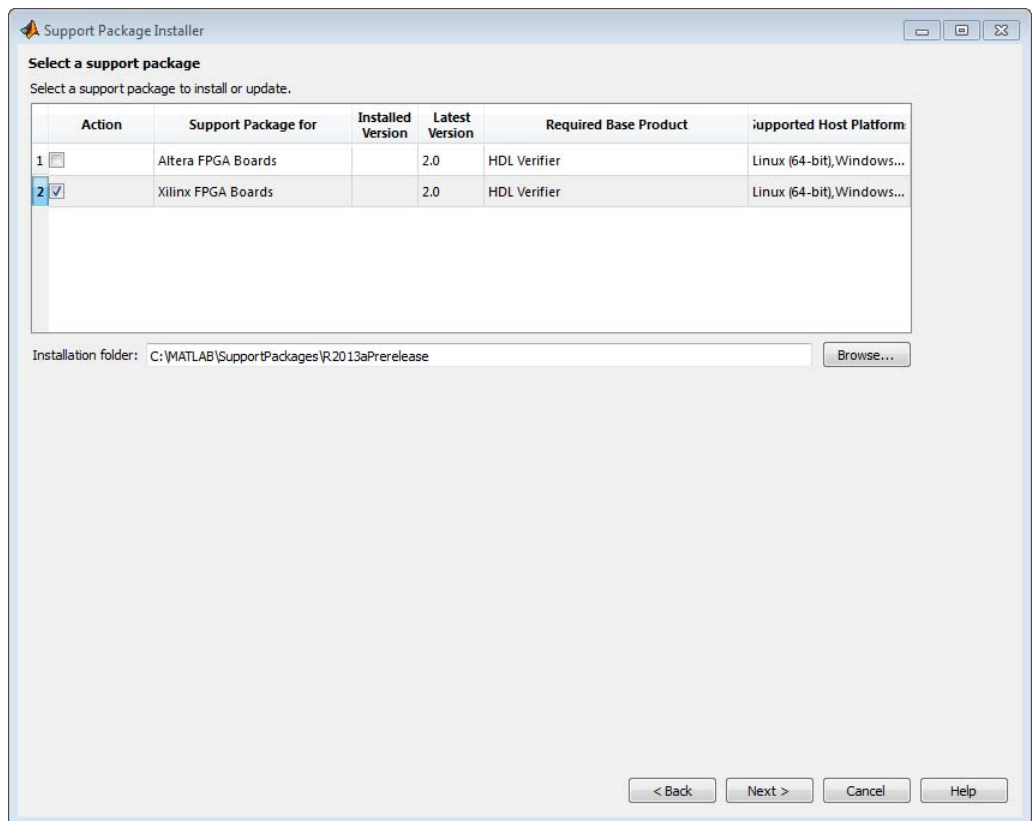
Compatibility Considerations

You no longer require Embedded Coder to generate Transaction Level Models with HDL Verifier.

Support Package for FPGA-in-the-Loop

All FPGA boards supported by FPGA-in-the-Loop are now available via download with the Support Package Installer. You can choose to download all supported Altera® boards or all supported Xilinx® boards, or both.

When you are using the FPGA Board Manager, select **Get More Boards** to start the Support Package Installer with the FPGA board download packages already displayed. You can also access the installer through the FIL Wizard (Get more boards). The installer guides you through selecting and installing the board support package. After the installer has completed the download, you can access any supported board through the FPGA Board Manager or the FIL Wizard.



Code Generation for FIL Simulation Block

With Release R2013a, you can generate code for the FIL Simulation block.

Updates to supported software and boards

Compatibility Considerations: Yes

- “Software updates” on page 7
- “Board additions” on page 7

Software updates

FPGA Verification

- Xilinx ISE 14.2
- Altera Quartus™ II 12.0

TLM Generation

- Compilers:
 - Visual Studio®: VS2005, VS2008, VS2010
 - gcc 4.4.6
- SystemC:
 - SystemC 2.3.0 (TLM included)

Board additions

- Altera DSP Stratix V

For a list of supported boards and device families, see “Supported EDA Tools”. To add a custom board for use with FIL, see “Create Custom FPGA Board Definition”.

Compatibility Considerations

Xilinx does not ship the Digilent plugin with ISE 14.2. To get the plugin, see the Digilent plugin and related software download page on the Digilent web site.

HDL Verifier No Longer Supports Legacy FIL Programming Files

Compatibility Considerations: Yes

FPGA-in-the-Loop FPGA programming files generated using HDL Verifier versions older than 4.2 (current release) are not compatible with the current version of software.

Compatibility Considerations

FPGA programming files that were generated with version 4.1 or earlier of HDL Verifier are unusable with the current version of software (R2013a). You must regenerate these programming files using the FIL Wizard or HDL Workflow Advisor with the current release.

Functions and Function Elements Being Removed

Compatibility Considerations: Yes

Function or Function Element Name	What Happens When You Use The Function or Element?	Use This Instead	Compatibility Considerations
FrameBasedProcessing property	Warns	Sample mode or frame mode is automatically detected based on the size of the inputs during the step method execution.	In a future release, the use of any scripts containing this property will cause an error.
FPGA Automation pane in the Generate HDL dialog box	Warns		In a future release, the FPGA Automation pane will be removed.

R2012b

Version: 4.1
New Features: Yes
Bug Fixes: Yes

Custom board APIs for FPGA-in-the-loop

New FPGA Board Manager allows you to add custom board information so that you can use FIL simulation with an FPGA board that is not one of the pre-registered boards. See “Create Custom FPGA Board Definition”.

System object for FPGA-in-the-Loop

FIL System object™ for FIL simulation between FPGA and MATLAB. The `hdlverifier.FILSimulation` System object can be generated only with the FIL Wizard. See .

100 Base-T Ethernet support for FPGA-in-the-loop block

HDL Verifier supports FPGA boards that have 100 Mbit/sec Ethernet PHY. The software will automatically detect the configuration of the PHY chip and employ the appropriate interface in the FPGA as necessary for FIL simulation.

Automatic verification with cosimulation using HDL Coder

With the HDL Coder™ HDL Workflow Advisor, you can automatically verify using your Simulink test bench with the new verification step **Run Cosimulation TestBench**. During verification, the HDL Workflow Advisor and HDL Verifier verify the generated HDL using cosimulation between the HDL Simulator and the Simulink test bench. See “Automatic Verification”.

Updates to supported software and boards

- “Software updates” on page 16
- “Board additions” on page 16

Software updates

- ModelSim 10.1a, 10.0c, and 6.6d
- Cadence Incisive® 11.10-s005
- Xilinx ISE 13.4

Board additions

- Altera Nios II Embedded Evaluation Kit, Cyclone III Edition

For a full list of preregistered boards, see “Supported FPGA Device Families for Board Customization”. To add a custom board for use with FIL, see “Create Custom FPGA Board Definition”.

R2012a

Version: 4.0
New Features: Yes
Bug Fixes: Yes

EDA Simulator Link Is Now HDL Verifier

Effective R2012a, EDA Simulator Link is now HDL Verifier.

FPGA-in-the-Loop for Altera Boards

FPGA-in-the-Loop now supports Altera FPGA design software and the following Altera development kits and boards:

- Altera Arria II GX FPGA development kit
- Altera Cyclone III FPGA development kit
- Altera Cyclone IV GX FPGA development kit
- Altera DE2-115 development and education board

See Required Products, Performing FPGA-in-the-Loop.

System Object for HDL Cosimulation with MATLAB, with Automatic System Object Generation

The HDL cosimulation System object provides integrated HDL cosimulation with MATLAB. When you use this workflow to cosimulate MATLAB and HDL code, you gain the following benefits of using the System object:

- Control all aspect of the cosimulation from MATLAB.
- Easily configure all test bench parameters.
- Remove need for multiple function calls.
- Create System object automatically from existing HDL code (see “Automatic System Object Generation with CosimWizard” on page 20).

The HDL cosimulation System object supports HDL cosimulation with both Mentor Graphics® ModelSim and Cadence Incisive. You can read more about the HDL cosimulation System object and its methods and properties in the HDL Cosimulation System Objects reference page.

Automatic System Object Generation with CosimWizard

Although you can hand code an HDL cosimulation System object, you can more easily create the System object automatically using existing HDL code and the HDL Cosimulation Wizard. This workflow also creates an HDL launch script for easier startup.

See [Creating a Function, System Object, or Block](#).

Use of FPGA Board as Source Block with FPGA-in-the-Loop

Effective R2012a, you can use the FPGA board as the source of stimuli in Simulink. Only one output is required. This feature enables high speed generation and processing of test stimulus with results brought back to Simulink for analysis.

See the example “Algorithm Verification with FIL Source Block”.

HDL Regression Testing with Simulink Design Verifier

You can now perform successive simulation runs without restarting the HDL simulator. This enhancement allows uses of automatically generated test cases, from the original behavioral model, generated from Simulink Design Verifier™. Such regression testing can achieve complete model and HDL code coverage.

Previously, commands issued in the Tcl startup file were executed only once, when the HDL simulator was started. Now, Tcl commands in the Simulation pane of the HDL Cosimulation block are stored with the block and are issued with each new simulation run. You do not have to reissue the commands in the HDL simulator.

See the example “Generating HDL Code Coverage Using Simulink and ModelSim”.

New Examples for R2012a

- HDL Cosimulation with MATLAB System object:
 - Cosimulation Wizard for MATLAB System object
 - Verifying Viterbi Decoder Using MATLAB System object and Cadence Incisive
 - Verifying Viterbi Decoder Using MATLAB System object and Mentor Graphics ModelSim
- Accelerate Algorithm Verification with a FIL Source Block
- Generating HDL Code Coverage Using Simulink and Mentor Graphics ModelSim
- FIL Demos Updated for Altera Workflow

HDL Verifier Supported Software and System Updates

The HDL Verifier supported software updates for this release are listed in the following sections.

See Required Products for a complete listing of supported products.

HDL Cosimulation

- Support for ModelSim 10.0c added
- No change to supported Cadence Incisive versions

FPGA-in-the-Loop

- Altera Quartus 11.0
- No change to supported Xilinx Design Suite versions

Functions and Function Elements Being Removed

Compatibility Considerations: Yes

Function or Function Element Name	What Happens When You Use The Function or Element?	Use This Instead	Compatibility Considerations
FPGA Automation in Configuration Parameters or Model Explorer	You cannot access this feature	Use the HDL Workflow Advisor.	Use replacement workflow.
fpgamodelsetup	Errors	Use the HDL Workflow Advisor	Use replacement workflow.
makefpgaproject	Errors	Use the HDL Workflow Advisor	Use replacement workflow.
configuremodelsim	Errors	vsim	Use replacement function.
wrapverilog	Errors	Wrapping Verilog code is no longer required.	

R2011b

Version: 3.4
New Features: Yes
Bug Fixes: Yes

FPGA-in-the-Loop Workflow in HDL Coder HDL Workflow Advisor

FPGA-in-the-Loop (FIL) is available using the HDL Coder HDL Workflow Advisor. You can verify FPGA designs with FIL as part of the HDL Workflow Advisor workflow, which will create the FPGA programming file and download it to your selected development board. See HDL Coder documentation for details.

FPGA-in-the-Loop Updates

This release removes previous limitations and now supports:

- Arbitrary vectors. Limitations on input and output signal size in FIL have been removed.
- Variable step solvers
- ode45 solvers and model referencing

Conversion of Error and Warning Message Identifiers

Compatibility Considerations: Yes

For R2011b, EDA Simulator Link™ error and warning message identifiers have changed.

Compatibility Considerations

If you have scripts or functions that use message identifiers that changed, you must update the code to use the new identifiers. Typically, message identifiers are used to turn off specific warning messages.

For example, the `edalink:filWizard:NotString` identifier has changed to `edalink:filWizard:NotString`. If your code checks for `edalink:filWizard:NotString`, you must update it to check for `edalink:filWizard:NotString` instead.

To determine the identifier for a warning that appears at the MATLAB prompt, run the following command after you see the warning:

```
[MSG,MSGID] = lastwarn;
```

This command saves the message identifier to the variable `MSGID`.

Note Warning messages indicate a potential issue with your model or code. While you can turn off a warning, a suggested alternative is to change your model or code so it does not generate warnings.

EDA Simulator Link Supported Software and System Updates

EDA Simulator Link supported software updates for this release include:

- ModelSim SE 10.0a, 6.6d, 6.5f
- ModelSim PE 10.0a, 6.6d, 6.5f
- ModelSim DE 10.0a (Windows® 32 only)
- Questa® 10.0a
- Cadence® IES 10.2-s040
- Cadence IES 9.2-s014
- Cadence IUS 8.2-s009
- Xilinx ISE 13.1

See Required Products.

Functions and Function Elements Being Removed

Compatibility Considerations: Yes

Function or Function Element Name	What Happens When you use the Function or Element?	Use This Instead	Compatibility Considerations
FPGA hardware-in-the-loop via the EDA	Errors	filWizard or FIL in the HDL	Use replacement function
FPGA Automation in Configuration Parameters or	Warns	Use the HDL Workflow	Use replacement workflow
configuremodelsim	Errors	vsim	Use replacement function
launchDiscovery	Errors	Support for Synopsys® Discovery™ has been removed.	You must remove the launchDiscovery command from any scripts or programming files that contain it.
HDL Cosimulation block—Discovery	Errors	Support for Synopsys Discovery	Remove or replace the Discovery HDL

Function or Function Element Name	What Happens When you use the Function or Element?	Use This Instead	Compatibility Considerations
		has been removed.	Cosimulation block in your Simulink models.

R2011a

Version: 3.3
New Features: Yes
Bug Fixes: Yes

FPGA-in-the-Loop Simulation

This release provides the capability for verification of FPGA designs with FPGA-in-the-Loop (FIL) simulation. The FIL Wizard, using HDL files that you provide, creates all the FPGA programming files and downloads them to a development board. It also provides you with a FIL block to insert into your existing model so that you can then run and test your FPGA implementation on the development board using Simulink. See [Generating a FIL Simulation Block](#) for details.

EDA Simulator Link tested FIL simulation with: Xilinx ISE 12.1; Supports Windows 32, Windows 64, Linux[®] 32, Linux 64.

Multiple Cosimulation Sessions Support with Parallel Computing

You can use the EDA Simulator Link and Parallel Computing Toolbox™ products together for up to eight cosimulation sessions on local machine. Use MATLAB Distributed Computing Server™ to farm out sessions to any number of other computers or to run more than eight sessions on a local machine.

Refer to the Parallel Computing Toolbox and the MATLAB Distributed Computing Server documentation for details and examples of using parallel computing with MATLAB and Simulink.

New User Guide Section for Using HDL Instance Object with Test Bench and Component Functions

Expanded documentation helps you learn how to use the `use_instance_obj` argument for MATLAB functions `matlabcp` and `matlabtb`. You can use this feature to pass an HDL instance object to the function as an argument. In previously releases, the `iport`, `oport`, `tnext`, `tnow`, and `portinfo` arguments of the MATLAB function definition served this purpose. With this feature, `matlabcp` and `matlabtb` function callbacks get the HDL instance object passed in: to hold state, provide read/write access protection for signals, and allow you to add state as you wish.

See [Writing Functions Using the HDL Instance Object](#) for details.

EDA Cosimulation Assistant Name Change to Cosimulation Wizard

Compatibility Considerations: Yes

The feature name "EDA Cosimulation Assistant" has been changed to "Cosimulation Wizard". The function used to launch the wizard has changed also. The function `edaCosimAssist` will be removed in a future release. Although `edaCosimAssist` is supported for backward compatibility, you should use function `cosimWizard` instead. See [Creating a Function, System Object, or Block](#).

Compatibility Considerations

Replace all existing instances of `edaCosimAssist` with `cosimWizard`.

EDA Simulator Link Supported Software and System Updates

- For FPGA Automation (with Simulink or Filter Design HDL Coder™):
 - Tested with Xilinx ISE 12.1
 - Added Windows 64 support
- For HDL Cosimulation:
 - ModelSim SE 6.6c, 6.5f, 6.4g
 - ModelSim PE 6.6c, 6.5f, 6.4g
 - ModelSim DE 6.6c (Windows 32 only)
 - Questa 6.6c
 - Support for Synopsys Discovery will be removed in a future release.
- Windows 64 Support Added for TLM Component Generation

Functions and Function Elements Being Removed

Compatibility Considerations: Yes

Function or Function Element Name	What Happens When you use the Function or Element?	Use This Instead	Compatibility Considerations
edaCosimAssist	Still runs	cosimWizard	Replace all existing instances of edaCosimAssist with cosimWizard.
launchDiscovery	Warns		Support for Synopsys Discovery will be removed in a future release.
HDL Cosimulation block—Discovery	Warns		Support for Synopsys Discovery will be removed in a future release.
FPGA hardware-in-the-loop	Warns	FPGA-in-the-Loop	Support for FPGA HIL will be removed in a future release.

R2010b

Version: 3.2
New Features: Yes
Bug Fixes: No

HDL Cosimulation Updates

Compatibility Considerations: Yes

- “EDA Cosimulation Assistant Creates Blocks and Functions from Existing HDL Code” on page 44
- “Updated Timescales Pane Offers New Options for Simulation Timescale Factoring” on page 44
- “To VCD File Block Supports Simulation Using Rapid Accelerator Mode” on page 44
- “EDA Simulator Link Supports ModelSim DE” on page 45
- “EDA Simulator Link Supports Cosimulation on 64-Bit Windows” on page 45
- “HDL Cosimulation Support for Synopsys Updated” on page 45
- “Zero Value of First Output for All Signals Corrected” on page 45

EDA Cosimulation Assistant Creates Blocks and Functions from Existing HDL Code

Get started quickly using existing HDL code and the EDA Cosimulation Assistant. This tool will guide you through the steps to create a test bench or component function for cosimulation with MATLAB or an HDL Cosimulation block for cosimulation with Simulink. See [Generate HDL Cosimulation Interfaces from Existing HDL Code](#).

Updated Timescales Pane Offers New Options for Simulation Timescale Factoring

The updated timescale features allows you to choose when EDA Simulator Link software should calculate a timescale for you. In addition, you can make changes to the calculated timescale with an interactive GUI. See the [HDL Cosimulation block reference](#) for more information.

To VCD File Block Supports Simulation Using Rapid Accelerator Mode

To VCD File block now supports simulation using Rapid Accelerator mode. Select **Simulation > Rapid Accelerator Mode** in the model window before

beginning cosimulation. See the To VCD File block reference for more information about this feature and block settings.

EDA Simulator Link Supports ModelSim DE

EDA Simulator Link software now supports ModelSim DE 6.6a (for Windows only). See Product Requirements for more information on supported products.

EDA Simulator Link Supports Cosimulation on 64-Bit Windows

This release adds support for Windows 64-bit machines. See Product Requirements for more information on supported products.

HDL Cosimulation Support for Synopsys Updated

With the release of R2010b, EDA Simulator Link software now supports VCS MXi. The software no longer supports VCX MX.

Compatibility Considerations

Attempts to cosimulate with VCX MX will result in errors.

Zero Value of First Output for All Signals Corrected

Previously, the first output value of all signals in the HDL code was set to zero in Simulink (unless you used direct feedthrough, which works as expected). Effective this release, the output value of all signals now pass from the HDL simulator to Simulink as expected.

Compatibility Considerations

You will no longer see zero as the first output value of all signals in Simulink. You may need to modify your code or procedures to accommodate the corrected behavior.

FPGA Automation Updates

- “FPGA Project Generation with MATLAB and Filter Design HDL Coder” on page 46
- “Clock Module Generation Now Supports Verilog” on page 46

FPGA Project Generation with MATLAB and Filter Design HDL Coder

You can create Xilinx ISE projects from Filter Design HDL Coder and MATLAB. From the Filter Design & Analysis Tool GUI, select **Targets > Generate HDL**. Select the **FPGA Automation** tab. Use context-sensitive help to assist you in setting project generation options.

The software now supports FPGA project generation with MATLAB and Filter Design HDL Coder on 32-bit Windows systems and on 32- and 64-bit Linux systems.

See FPGA Project Generation with Xilinx to get started.

Clock Module Generation Now Supports Verilog

The limitation for DCM design containing only VHDL code has been removed. You may select Verilog on the HDL Coder pane or the Generate HDL pane (in Filter Design HDL Coder) when you specify options for FPGA project generation.

TLM Generation Updates

- “Single Source and Sink Blocks Now Supported” on page 47
- “New Algorithm Processing Options” on page 47
- “Temporal Decoupling Added to Generated TLM and Test Bench” on page 47

Single Source and Sink Blocks Now Supported

This release removes the previous limitation that designs under generation must contain both inputs and outputs. Your design now may have only source blocks or only sink blocks.

New Algorithm Processing Options

Choose the type of function execution trigger you want to use in the generated TLM component—SystemC thread or callback. Use a SystemC thread for a more realistic simulation (at the expense of time) and use a callback for faster execution (at the expense of accuracy).

Temporal Decoupling Added to Generated TLM and Test Bench

This release includes complete temporal decoupling implementation with quantum for faster processing for generated TLM and test bench.

R2010a

Version: 3.1
New Features: Yes
Bug Fixes: No

Support for Latest Synopsys Discovery Release

EDA Simulator Link now supports the latest Synopsys release. See the requirements page on the MathWorks Web site for specific platforms supported and detailed information about the software and hardware required to use EDA Simulator Link software with the current release.

Enable Direct Feedthrough for HDL Designs with Pure Combinational Datapaths

The HDL Cosimulation block now supports *direct feedthrough*, which means that the output is controlled directly by the value of an input port. The input value change propagates to the output ports in zero time, thus eliminating one output-sample delay for HDL designs with pure combinational logic datapaths. This feature eliminates the need to modify the test bench portion of Simulink to compensate for cosimulation block delay.

New Functions for HDL Simulator Client Communication

A new function, `notifyMatlabServer`, allows you to send HDL simulator event and process IDs to MATLAB server. Another new function, `waitForHdlClient`, waits to begin processing until the specified event ID is obtained or a user-specified time-out occurs.

Batch, CLI, and GUI Mode Support Added for Cosimulation with HDL Simulators

You can execute cosimulation in batch mode for background processing or CLI mode for ease in debugging.

Use Same MATLAB Function for Multiple HDL Instances

This release adds a new argument, `use_instance_obj`, to the MATLAB functions `matlabcp` and `matlabtb`. This feature replaces the `iport`, `oport`, `tnext`, `tnow`, and `portinfo` arguments of the MATLAB function definition with an HDL instance object passed to the function as an argument. With this feature, `matlabcp` and `matlabtb` function callbacks get the HDL instance object after it has passed into hold state. They also provide read/write access protection for signals and allow you to add state as you wish.

With this feature you gain the following advantages:

- You can use the same MATLAB function to represent behavior for different instances of the same module in HDL without need to create one-off wrapper functions.
- You no longer need special "portinfo" argument on first invocation.
- You no longer need to use persistent or global variables.
- You receive better feedback and protections on reading/writing of signals.
- You can use object fields to identify the instance path and whether the call comes from a component or test bench function.
- You can use the field argument to pass user-defined arguments from the `matlabcp` or `matlabtb` instantiation on the HDL side to the function callbacks.

The new argument, `-use_instance_obj`, is identical for both `matlabcp` and `matlabtb`. See the Function Reference for `matlabcp` and `matlabtb` for instructions in using this new function argument.

Generating Transaction Level Models for Use with Virtual Platforms

- Export of Simulink algorithm models as OSCI TLM 2.0 components
- Generation of standalone SystemC test bench for generated TLM 2.0 component

Limitations The design under generation must contain both inputs and outputs. Designs that only have inputs or only have outputs (sink or source blocks) are not supported in this release. If you do not include both, EDA Simulator Link displays an error message and discontinues code generation.

Specializing FPGA Implementations

Generation of Xilinx ISE projects for FPGA designs

R2009b

Version: 3.0
New Features: Yes
Bug Fixes: No

EDA Simulator Link DS, EDA Simulator Link IN, and EDA Simulator Link MQ Merge

As of R2009b, EDA Simulator Link DS™, EDA Simulator Link IN™, and EDA Simulator Link MQ™ functionality are merged into a new product, EDA Simulator Link. These individual products are no longer available.